REMARKS

Claims 51-77 are pending in the present application. Claims 51-61 stand rejected under 35 U.S.C. §103(a) for obviousness over U.S. Patent No. 5,672,525 to Pan (the Pan '525 patent) in combination with U.S. Patent No. 5,705,409 to Witek (the Witek patent) and U.S. Patent No. 5,750,435 to Pan (the Pan '435 patent). Claims 51-75 stand revisionally rejected under the judicially-created doctrine of obviousness-type double patenting over claims 22-30 of co-pending application number 08/993,663.

Applicants traverse the rejections and urge allowance of the present application.

Referring to the 35 U.S.C. §103 rejections, the teachings of the references do not support an obviousness rejection of the claims. An obviousness rejection requires consideration of all the elements of the claimed invention. Further, all such elements must be shown to be suggested by the prior art when making a rejection based upon obviousness under 35 U.S.C. §103(a). *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1987).

Independent claim 51 defines a method of forming a transistor gate comprising, in part, providing at least one of fluorine or chlorine within a gate oxide layer and forming a gate proximate the gate oxide layer after the providing. The subject matter of claim 51 is not shown or suggested in the prior art of record.

None of the prior art references, taken alone or in combination, teach or suggest providing at least one of fluorine and chlorine within a gate oxide layer, and forming a gate proximate the gate oxide layer *after the providing* as claimed.

Referring initially to the Pan '525 patent, such clearly discloses with reference to Figs. 1C-1E the formation of the gate prior to fluorination of layer 18. Referring to the Pan '435 patent, such clearly discloses in Figs. 1A-1B the formation of gate electrode 16 and subsequent implantation of fluorine ions in Fig. 1B following the formation of gate electrode 16. Referring to Fig. 8 and Fig. 9 of the Witek patent, such fails to teach or suggest the formation of a gate oxide layer over a semiconductive substrate in combination with forming a gate proximate the gate oxide layer after the providing as claimed.

Accordingly, the teachings of the Pan '525 patent, the Pan '435 patent and the Witek patent, taken singularly or in combination, fail to teach or suggest limitations of claim 51. As not one of the cited references discloses such recited limitations, it is inconceivable that the references could, singularly or in any combination, suggest such recited limitation. Claim 51 defines patentable subject matter over the prior art of record.

Claims 52-54 and claims 76-77 depend from independent claim 51 and therefore are in condition for allowance for the reasons discussed above with respect to claim 51 as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to independent claim 55, a method of forming a transistor gate is defined comprising, in part, forming a gate and a gate oxide layer in overlapping relation, the gate oxide layer having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate; and concentrating at least one of chlorine or fluorine in the gate oxide layer having the outwardly exposed opposing edges and within the overlap. The subject matter of independent claim 55 is not shown or suggested in the prior art of record.

None of the prior art references, taken alone or in combination, teach or suggest forming a gate oxide layer having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate, and concentrating at least one of chlorine or fluorine in the gate oxide layer *having the outwardly exposed opposing edges* as claimed.

Referring initially to the Pan '525 patent, the structure of Figs. 1A-1J and Figs. 2-5 fails to teach or suggest the gate oxide having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate and concentrating at least one of chlorine or fluorine in the gate oxide layer having the outwardly exposed opposing edges. As described in col. 5, lines 6-8, of the Pan '525 patent, the structure of Fig. 1C further receives a blanket thin silicon oxide dielectric layer 18 to provide the structure of Fig. 1D. Fluorination thereafter occurs with respect to Fig. 1E. Accordingly, the Pan '525 patent fails to teach or suggest concentrating at least one of chlorine or fluorine in

the gate oxide layer having the outwardly exposed opposing edges as claimed.

Further, the Pan '435 patent fails to teach or suggest the formation of the gate oxide layer having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate. Referring to Figs. 1A-1E of the Pan '435 patent, all such disclosed structures additionally fail to teach or suggest concentrating at least one of chlorine or fluorine in the gate oxide layer having the outwardly exposed opposing edges as claimed.

In addition, the disclosed structures of the Witek patent fail to teach or suggest the formation of the gate and the gate oxide layer as claimed having outwardly exposed opposing edges laterally aligned with the edges of the gate and concentrating at least one of chlorine or fluorine in the gate oxide layer having the outwardly exposed opposing edges.

Accordingly, the teachings of the Pan '525 patent, the Pan '435 patent and the Witek patent, taken alone or in combination, fail to teach or suggest positively-defined limitations of independent claim 55. Accordingly, claim 55 is patentable over the prior art of record.

Claims 56-61 depend from independent claim 55 and therefore are in condition for allowance for the reasons discussed above with respect to claim 55 as well as for their own respective features which are neither shown nor suggested by the cited art.

With regards to the double patenting rejection, application serial number 08/993,663 has been abandoned by Applicants and the claims thereof are currently being prosecuted in application serial number 09/332,255. Accordingly, it is believed that the obviousness-type double patenting rejection is improper in view of the abandonment of application serial number 08/993,663.

Applicants have not yet received Forms PTO-1449 submitted to the Patent Office with Information Disclosure Statements on April 14, 1999, December 13, 1999 and January 27, 2000 with the initials of the Examiner indicating full consideration of the references thereon. Applicants respectfully request full consideration of such references, the initialling of all references on the respective Forms PTO-1449, and the forwarding of such initialled Forms PTO-1449 to the undersigned.

Applicants respectfully request allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 2/9/00

By: _____
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